In the Claims:

1. (currently amended) A built-in self-test circuit for testing a data processing circuit arranged to serialize and deserialize received parallel data into processed parallel data, the built-in self-test circuit comprising:

a transmit register that transmits parallel data to the data processing circuit for processing the parallel data into processed parallel data;

a receive register that receives the processed parallel data from the data processing circuit; and

an error detector coupled to the transmit register for receiving the transmitted parallel data from the transmit register and to the receive register for receiving the processed parallel data and that detects errors in the processed parallel data,

the transmit register being a programmable transmit register that comprises a register array and that transmits parallel data having programmably varying characteristics by generating a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array.

2. (original) The built-in self-test circuit of claim 1 wherein the programmably varying characteristics includes data sequence.

3. (original) The built-in self-test circuit of claim 1 wherein the programmably varying characteristics include data sequence length.

4. (original) The built-in self-test circuit of claim 1 wherein the programmably varying characteristics include data sequence and data length.

5. (original) The built-in self-test circuit of claim 1 wherein the programmable transmit register comprises a programmable bit sequence generator that generates the transmitted data.

6. (currently amended) The built-in self-test circuit of claim 1 wherein the programmable transmit register further comprises a shift register.

7. (currently amended) The built-in self-test circuit of claim 1 wherein the programmable transmit register further comprises a pseudo random counter.

8. Cancelled.

9. Cancelled.

10. Cancelled.

11. (original) The built-in self-test circuit of claim 1 wherein the error detector comprises a comparator.

12. (currently amended) A built-in self-test circuit for testing a data processing circuit arranged to serialize and deserialize received parallel data into processed parallel data comprising:

a programmable transmit register that transmits parallel data having programmably varying data sequences to the data processing circuit for processing the parallel data into processed parallel data, the programmable transmit register comprising a register array and generating a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array;

a receive register that receives the processed parallel data from the data processing circuit; and

an error detector coupled to the transmit register for receiving the transmitted parallel data from the transmit register and to the receive register for receiving the processed parallel data and that detects errors in the processed parallel data.

13. (currently amended) The built-in self-test circuit of claim ~~1~~ 12 wherein the programmably varying data sequences have programmably varying data sequence lengths.

14. (original) The built-in self-test circuit of claim 12 wherein the programmable transmit register comprises a programmable bit sequence generator.

15. (currently amended) The built-in self-test circuit of claim 12 wherein the programmable transmit register further comprises a pseudo random counter.

16. Cancelled.

17. Cancelled.

18. (currently amended) An integrated circuit comprising:

a data processing circuit arranged to serialize and deserialize received parallel data into processed parallel data; and

a built-in self-test circuit that includes,

a programmable transmit register that transmits parallel data having programmably varying characteristics to the data processing circuit for processing parallel data into processed parallel data, the programmable transmit register comprising a register array and generating a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array;

a receive register that receives the processed parallel data from the data processing circuit; and

an error detector coupled to the transmit register for receiving the transmitted parallel data from the transmit register and to the receive register for receiving the processed parallel data and that detects errors in the processed data.

19. (currently amended) The integrated circuit of claim 18 wherein the programmable transmit register further comprises a pseudo random counter.

20. Cancelled.

21. (currently amended) In an integrated circuit, a method comprising:

generating programmably varying parallel data by generating a programmable combination of a plurality of bit sequences;

transmitting the programmably varying parallel data to a data processing circuit;

causing the data processing circuit to serialize and deserialize the transmitted data to produce processed parallel data; and

testing the processed parallel data for errors by comparing the transmitted data to the processed parallel data.

22. (previously presented) The method of claim 21 wherein the transmitting step includes providing varying data sequences in the data.

23. (previously presented) The method of claim 21 wherein the transmitting step includes providing varying data sequence length of the data.

24. Cancelled.